Amendments to the Claims

1-60. (Canceled).

61. (Currently Amended) A method of fabricating an integrated optical device, said method comprising:

providing a support wafer defining an electrode support surface;

forming an electrode pattern over said electrode support surface of said support wafer;

forming a non-polymeric buffer layer on at least a portion of said electrode pattern and over at least a portion of said support wafer;

forming a non-polymeric, silica-based waveguide core material layer over said non-polymeric buffer layer;

removing portions of said core material layer to define a non-polymeric waveguide core and a pair of cladding containment regions extending along opposite sides of said non-polymeric waveguide core in a direction substantially parallel to a longitudinal dimension of said non-polymeric waveguide core, wherein each of said pair of cladding containment regions is defined between distinct pairs of opposing side walls and the waveguide core is disposed between the cladding containment regions such that each side of the waveguide core forms a side wall of a cladding containment region; and

positioning a polymeric cladding material within at least a substantial portion of said pair of cladding containment regions so as to place said polymeric cladding material in optical communication with said non-polymeric waveguide core such that said non-polymeric buffer layer, said polymeric cladding material, and said non-polymeric waveguide core define an optically-clad waveguide core, wherein at least one of said cladding material and said waveguide core are configured such that a control signal applied to said electrode pattern alters a transmission characteristic of an optical signal propagating along said waveguide core.

62. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said electrode pattern, said buffer layer, and said waveguide core are formed such that said electrode pattern is embedded in said device beneath said waveguide core.

63. (Currently amended) A method of fabricating an integrated optical device, said method comprising:

providing a support wafer defining an electrode support surface;

forming an electrode pattern over said electrode support surface of said support wafer wherein said electrode pattern is formed so as to define at least two electrically isolated control electrodes over said electrode support surface;

forming a non-polymeric buffer layer on at least a portion of said electrode pattern and over at least a portion of said support wafer;

forming a waveguide core material layer over said non-polymeric buffer layer;

removing portions of said core material layer to define a waveguide core and a pair of cladding containment regions extending along opposite sides of said waveguide core in a direction substantially parallel to a longitudinal dimension of said waveguide core, wherein each of said pair of cladding containment regions is defined between distinct pairs of opposing side walls and the waveguide core is disposed between the cladding containment regions such that each side of the waveguide core forms a side wall of a cladding containment region; and

positioning a cladding material within at least a substantial portion of said pair of cladding containment regions so as to place said cladding material in optical communication with said waveguide core such that said buffer layer, said cladding material, and said waveguide core define an optically-clad waveguide core, wherein an electrically insulative barrier layer is formed over said control electrodes prior to positioning said cladding material in optical communication with said waveguide core and at least one of said cladding material and said waveguide core are configured such that a control signal applied to said electrode pattern alters a transmission characteristic of an optical signal propagating along said waveguide core.

64. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 63 wherein said electrically insulative barrier layer is formed over said control electrodes as a layer of silica.

65. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 63 wherein a sufficient portion of said buffer layer formed over said electrode pattern is maintained prior to positioning said cladding material in optical communication with said waveguide core so as to form said electrically insulative barrier between said isolated control electrodes.

66. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 63 wherein said electrode pattern is formed such that said control electrodes are substantially co-planar.

67. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said electrode pattern defines at least two electrically isolated control electrodes and said waveguide core is formed through a process by which said position of said core in a plane offset from and generally parallel to a plane occupied by said control electrodes is controlled relative to respective positions of said control electrodes in said control electrode plane.

68. (Withdrawn) A method of fabricating an integrated optical device as claimed in claim 61 further comprising the step of positioning an additional electrode pattern above said electrode pattern formed over said electrode support surface of said support wafer.

69. (Withdrawn) A method of fabricating an integrated optical device as claimed in claim 68 wherein said additional electrode pattern comprises a single control electrode substantially aligned with said waveguide core.

70. (Withdrawn) A method of fabricating an integrated optical device as claimed in claim 68 wherein said additional electrode pattern comprises a single control electrode offset along one side of said waveguide core and said electrode pattern formed over said electrode support surface of said support wafer comprises a single control electrode offset along an opposite side of said waveguide core.

71. (Withdrawn) A method of fabricating an integrated optical device as claimed in claim 70 wherein said single control electrode offset along one side of said waveguide core defines a thickness sufficient to extend alongside a substantial portion of said waveguide core.

72. (Withdrawn) A method of fabricating an integrated optical device as claimed in claim 70 wherein said additional electrode pattern comprises an additional single control electrode offset along said opposite side of said waveguide core above said electrode pattern formed over said electrode support surface of said support wafer.

73. (Withdrawn) A method of fabricating an integrated optical device as claimed in claim 68 wherein:

said additional electrode pattern comprises a single control electrode offset along one side of said waveguide core and an additional single control electrode offset along an opposite side of said waveguide core; and

said electrode pattern formed over said electrode support surface of said support wafer comprises a single control electrode substantially aligned with said waveguide core.

74. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said electrode pattern comprises at least one material selected from Au, Pt, Cr, Ta, Ti, indium tin oxide, and combinations thereof.

75. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said electrode pattern comprises Cr.

76. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said electrode pattern comprises a conductive material characterized by a melting point of at least about 1500°C.

77. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said electrode pattern comprises first and second conductive layers, said first conductive layer having relatively enhanced adhesive properties and said second conductive layer having relatively enhanced conductive properties.

78. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said buffer layer is formed on said electrode pattern and said support wafer.

79. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said buffer layer is formed through a sol-gel process.

80. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 79 wherein said sol-gel process is characterized by a maximum processing temperature below about 400°C.

81. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said buffer layer is formed at a maximum processing temperature at least 500°C below a melting point of said buffer layer.

82. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said buffer layer is formed at a maximum processing temperature at least 500°C below a melting point of said electrode pattern.

83. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said buffer layer is formed through a plasma enhanced chemical vapor deposition process.

84. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 83 wherein said plasma enhanced chemical vapor deposition process is characterized by a maximum processing temperature below about 1000°C.

85. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said buffer layer comprises a silica-based buffer layer.

86. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 further comprising the act of removing portions of said buffer layer while leaving a sufficient amount of said buffer layer unremoved to define a remaining protective layer over said electrode pattern.

87. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said buffer layer comprises a material having a refractive index lower than a refractive index of said core material at an operating temperature and operating wavelength of said device.

88. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said buffer layer comprises a material characterized by a refractive index of between about 1.440 and about 1.450 at a selected operating temperature and operating wavelength of said device.

89. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said buffer layer comprises a material that is transmissive to light of at least one of the following wavelengths: about 1.3μm and about 1.55μm.

90. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said buffer layer comprises an electrically insulating, non-metallic material.

91. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said core layer comprises a material selected from polymers, silica, doped silica, and combinations thereof.

92. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said core layer is formed through a sol-gel process.

93. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said core layer comprises a material characterized by a refractive index of between about 1.450 and about 1.455 at a selected operating temperature and operating wavelength of said device.

94. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said portions of said core layer are removed through reactive ion etching.

95. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said waveguide core is formed by patterning said core material layer utilizing a waveguide mask.

96. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said cladding material comprises an electrooptic medium.

97. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 66 wherein said cladding material comprises an electrooptic chromophore.

98. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 96 wherein said cladding material comprises a medium dominated by the Pockels effect.

99. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 96 wherein said cladding material comprises a medium dominated by the Kerr effect.

100. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said cladding material is positioned in optical communication with said waveguide core through a sol-gel process.

101. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said cladding material is positioned in optical communication with said waveguide core as a polymeric solution.

102. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said cladding material is positioned in optical communication with said waveguide core as an aerosol of a polymeric solution.

103. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said cladding material is positioned in optical communication with said waveguide core as a vapor deposited polymer.

104. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said cladding material is positioned in optical communication with said waveguide core as an electro-deposited polymer.

105. (Currently amended) A method of fabricating an integrated optical device, said method comprising:

providing a support wafer defining an electrode support surface;

forming an electrode pattern over said electrode support surface of said support wafer;

forming a non-polymeric buffer layer on at least a portion of said electrode pattern and over at least a portion of said support wafer;

forming a waveguide core material layer over said non-polymeric buffer layer;

removing portions of said core material layer to define a waveguide core and a pair of cladding containment regions extending along opposite sides of said waveguide core in a direction substantially parallel to a longitudinal dimension of said waveguide core, wherein each of said pair of cladding containment regions is defined between distinct pairs of opposing side walls and the waveguide core is disposed between the cladding containment regions such that each side of the waveguide core forms a side wall of a cladding containment region; and

positioning a cladding material within at least a substantial portion of said pair of cladding containment regions so as to place said cladding material in optical communication with said waveguide core while a poling voltage is applied across said electrode pattern such that said buffer layer, said cladding material, and said waveguide core define an optically-clad waveguide core, wherein at least one of said cladding material and said waveguide core are configured such that a control signal applied to said electrode pattern alters a transmission characteristic of an optical signal propagating along said waveguide core.

106. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 105 wherein said poling voltage is maintained during curing, cross-linking, or thermo-setting of said cladding material.

107. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 105 wherein said cladding material comprises an electrooptic chromophore and said poling voltage is applied so as to be sufficient to orient said chromophore along a resulting electric field in said cladding material.

108. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 105 wherein an electrically insulative barrier layer is formed over said electrode pattern

prior to application of said poling voltage and said cladding material is positioned over said electrically insulating layer.

109. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said cladding material defines a thickness at least as large as a thickness defined by said core material layer.

110. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein further portions of said core material layer and said buffer layer are removed to define a pair of contact regions over said electrode pattern.

111. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 110 wherein said pair of contact regions is treated with hydrofluoric acid to remove residual material from said pair of contact regions.

112. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein portions of said buffer layer are removed to define a core material containment region.

113. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 112 wherein said core material containment region is defined prior to formation of said waveguide core material layer over said buffer layer.

114. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 61 wherein said waveguide core material layer is formed within a core material containment region defined by said buffer layer.

115. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 114 wherein said waveguide core material layer extends beyond said core material containment region defined by said buffer layer.

116. (Previously presented) A method of fabricating an integrated optical device as claimed in claim 114 wherein said waveguide core material layer is substantially confined within said core material containment region defined by said buffer layer.

117. (Currently amended) A method of fabricating an integrated optical device, said method comprising:

providing a support wafer defining an electrode support surface;

forming an electrode pattern over said electrode support surface of said support wafer;

forming a non-polymeric buffer layer on at least a portion of said electrode pattern and over at least a portion of said support wafer;

forming a waveguide core material layer over said non-polymeric buffer layer;

removing portions of said core material layer to define a waveguide core and a pair of cladding containment regions extending along opposite sides of said waveguide core in a direction substantially parallel to a longitudinal dimension of said waveguide core, wherein each of said pair of cladding containment regions is defined between distinct pairs of opposing side walls and the waveguide core is disposed between the cladding containment regions such that each side of the waveguide core forms a side wall of a cladding containment region; and

positioning a cladding material within at least a substantial portion of said pair of cladding containment regions so as to place said cladding material in optical communication with said waveguide core such that said buffer layer, said cladding material, and said waveguide core define an optically-clad waveguide core, wherein at least one of said cladding material and said waveguide core are configured such that a control signal applied to said electrode pattern alters a transmission characteristic of an optical signal propagating along said waveguide core.

118. (Canceled).

119. (Previously presented) A method of fabricating an integrated optical device, said method comprising:

providing a support wafer defining an electrode support surface;

forming an electrode pattern over said electrode support surface of said support wafer;

forming a buffer layer over said electrode pattern and said support wafer through a sol-gel process characterized by a maximum processing temperature below about 400°C;

forming a waveguide core and a pair of cladding containment regions over said buffer layer, wherein each of said pair of cladding containment regions is defined between distinct pairs of opposing side walls and the waveguide core is disposed between the cladding containment regions such that each side of the waveguide core forms a side wall of a cladding containment region; and

positioning a cladding material within at least a substantial portion of said pair of cladding containment regions so as to place said cladding material in optical communication with said waveguide core such that said buffer layer, said cladding material, and said waveguide core define an optically clad waveguide core, wherein at least one of said cladding material and said waveguide core are configured such that a control signal applied to said electrode pattern alters a transmission characteristic of an optical signal propagating along said waveguide core.

120. (Previously presented) An integrated optical device comprising:

a support wafer defining an electrode support surface;

an electrode pattern formed over said electrode support surface of said support wafer;

a non-polymeric buffer layer formed on at least a portion of said electrode pattern and over at least a portion of said support wafer;

a non-polymeric, silica-based waveguide core material layer formed over said buffer layer;

a polymeric cladding material positioned within at least a substantial portion of a pair of cladding containment regions so as to place said polymeric cladding material in optical communication with said non-polymeric waveguide core such that said non-polymeric buffer

layer, said polymeric cladding material, and said non-polymeric waveguide core define an optically-clad waveguide core, wherein each of said pair of cladding containment regions is defined between distinct pairs of opposing side walls and the waveguide core is disposed between the cladding containment regions such that each side of the waveguide core forms a side wall of a cladding containment region and at least one of said cladding material and said waveguide core are configured such that a control signal applied to said electrode pattern alters a transmission characteristic of an optical signal propagating along said waveguide core.